Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–III • EXAMINATION – WINTER 2013

Subject Code: X31101 Date: 18-12-2013

Subject Name: Advance Electronics

Time: 10.30 am - 01.30 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Draw the equivalent circuit of single stage CE amplifier at high frequency analysis. Derive expression for voltage gain and 3 dB frequency for such amplifier. **07**

(b) Explain the step response of an amplifier with necessary figures. **07**

Q.2 **(a)** What are the characteristics of an ideal op-amp? Derive gain of practical Inverting Operational amplifier. **07**

(b) Draw and Explain two stages cascaded amplifier and derive its equation for voltage gain. **07**

OR

(b) Three identical cascaded stages have an overall upper 3-dB frequency of 20 kHz and lower 3-dB frequency of 20 Hz. What are f_L and f_H of each stage? Assume non integrating stages. **07**

Q.3 **(a)** Derive the expression for input and output resistance for voltage series feedback topology. **07**

(b) State gain and phase margins and define stability criteria from these terms. **07**

OR

Q.3 **(a)** Explain briefly the following terms: (1) "Barkhausen criteria" for oscillator circuit. (2) Advantage of negative feedback **07**

(b) Draw the circuit diagram of current series feedback with transistor and derive the expression for gain, input resistance and output resistance. **07**

Q.4 **(a)** Design RC phase shift oscillator for the frequency of 1kHz by using n channel FET. **07**

(b) Consider differential amplifier which have first set of signals is $V_1 = +50\ \mu V$ and $V_2 = -50\ \mu V$ and the second set is $V_1 = +1050\ \mu V$ and $V_2 = +950\ \mu V$. (a) If the common mode rejection ratio is 100, calculate the percentage difference in output voltage obtained for the two set of signals (b) Repeat part (a) if CMRR = 10000. **07**

OR

Q.4 **(a)** Design Hartley oscillator for the frequency of 100 kHz by using Op-amp. **07**

Q.4 **(b)** Draw and explain emitter coupled differential amplifier. **07**

Q.5 **(a)** Describe the operation of successive approximation ADC with neat sketch. **07**

(b) List the logic family. Give comparisons of each of them. Also give the advantages and disadvantages of each logic families. **07**

OR

Q.5 **(a)** Draw and Explain R-2R DAC? Also give the advantages and disadvantages of R-2R Digital to Analog converter. **07**

(b) Draw and explain the classification of amplifier based on the magnitudes of the input and output impedances relative to the source and load impedances respectively. **07**

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