.Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 2715401 **Date: 07-01-2015**

Subject Name: ARM Processor Architecture and System Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **All the questions are related to ARM CPU LPC2148.**

Q.1 **(a)** Answer the following questions. **07**

1) How the barrel shifter can be used for multiplying two numbers?
2) What is the significance of FIQ mode in ARM CPU?
3) Explain any one instruction that helps to perform PUSH operation on stack.
4) What is literal pool of memory?
5) Mention an instruction to initialize a register R7 with an immediate 32 bit number 0x0068C234?
6) How can you know whether an ARM CPU is in THUMB mode or in ARM mode?
7) List out the three stages of pipeline in ARM CPU.

(b) Answer the following questions. **07**

1) List out the addressing modes related to memory access in ARM CPU with supporting examples of instructions.
2) Describe the benefits of five stage pipeline with explaining the operation done by ARM CPU in each of the five stages.

Q.2 **(a)** Write an ARM assembly language program to perform multiply and accumulate operation on all the elements of a given array of size 10 with each 32 bit number. Use a subroutine to implement this task. **07**

(b) How leaf and non leaf subroutines can be handled by an ARM CPU for appropriate return action? Describe in detail. **07**

OR

(b) Explain different types of pipeline stalls with their appropriate solutions. **07**

Q.3 **(a)** Explain the operation of Phase Locked Loop in LPC2148. How can you set the required CPU clock frequency? **07**

(b) Explain the requirement of a Watchdog Timer in Embedded System Design. Describe the Watchdog Reset Mode in LPC2148. **07**

OR

Q.3 **(a)** How can you use a Timer to generate a PWM wave in LPC2148? **07**

(b) Describe the Vector Interrupt Controller for serving vectored and non-vectored interrupt requests in LPC2148? **07**

Q.4 **(a)** Describe the ARM bus structure with requirement of several buses. **07**

(b) Answer the following questions. **07**

1) Explain the use of Global ADC Data Register in LPC2148.
2) Explain the special function registers to access Fast GPIO port pins.

OR

Q.4 **(a)** Describe the BURST mode of operation associated with ADC in LPC2148 with the help of an application. **07**

Q.4 **(b)** Answer the following questions. **07**

1) Explain the benefits of Memory Accelerator Module in LPC2148.
2) Explain the use of APB Divider in LPC2148.

Q.5 **(a)** Explain how you can set the desired baud rate for the implementation of serial communication using UART along with the importance of DLAB bit in LPC2148. **07**

(b) Describe the use of PWM modulator to generate PWM signals on port pins. **07**

OR

Q.5 **(a)** Explain the ñWired ANDò bus characteristics for CAN bus. Describe the requirements of such bus architecture. **07**

(b) Explain all the modes of operation associated with SPI bus in LPC 2148. **07**

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